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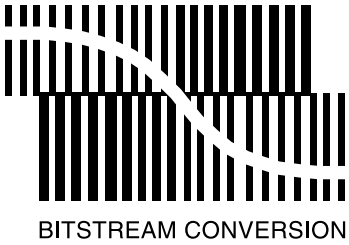
DATA SHEET



UDA1345TS
Economy audio CODEC

Preliminary specification
Supersedes data of 1999 Dec 02
File under Integrated Circuits, IC01

2000 Apr 18

Philips
Semiconductors

PHILIPS

FEATURES

General

- Low power consumption
- 2.4 V to 3.6 V power supply range with 3.0 V typical
- 5 V tolerant TTL compatible digital inputs
- 256, 384 and 512f_s system clock
- Supports sampling frequencies from 8 to 100 kHz
- Non-inverting ADC plus integrated high-pass filter to cancel DC offset
- The ADC supports 2 V (RMS) input signals
- Overload detector for easy record level control
- Separate power control for ADC and DAC
- Integrated digital interpolation filter plus non-inverting DAC
- Functions controllable either by L3 microcontroller interface or via static pins
- The UDA1345TS is pin and function compatible with the UDA1344TS
- Small package size (SSOP28).

Multiple format input interface

- I^2S-bus, MSB-justified up to 24 bits and LSB-justified 16, 18 and 20 bits format compatible
- Three combined data formats with MSB data output and LSB 16, 18 and 20 bits data input
- 1f_s input and output format data rate.

DAC digital sound processing

The sound processing features of the UDA1345TS can only be used in L3 microcontroller mode:

- Digital dB-linear volume control (low microcontroller load) via L3 microcontroller with 1 dB steps
- Digital de-emphasis for 32, 44.1 and 48 kHz
- Soft mute via cosine roll-off (in 1024 samples).

Note: in contrast to the UDA1344TS, the UDA1345TS does not have bass-boost and treble.

BITSTREAM CONVERSION

Advanced audio configuration

- Stereo single-ended input configuration
- Stereo line output (under microcontroller volume control), no post filter required
- High linearity, dynamic range and low distortion.

GENERAL DESCRIPTION

The UDA1345TS is a single-chip stereo Analog-to-Digital Converter (ADC) and Digital-to-Analog Converter (DAC) with signal processing features employing bitstream conversion techniques. The low power consumption and low voltage requirements make the device eminently suitable for use in low-voltage low-power portable digital audio equipment which incorporates recording and playback functions.

The UDA1345TS supports the I^2S-bus data format with word lengths of up to 24 bits, the MSB justified data format with word lengths of up to 20 bits and the LSB justified serial data format with word lengths of 16, 18 and 20 bits. The UDA1345TS also supports three combined data formats with MSB justified data output and LSB 16, 18 and 20 bits data input.

The UDA1345TS can be used either with static pin control or under L3 microcontroller interface. In L3 mode the UDA1345TS has basic sound features in playback mode such as de-emphasis, volume control and soft mute.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
UDA1345TS	SSOP28	plastic shrink small outline package; 28 leads; body width 5.3 mm	SOT341-1

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies						
$V_{DDA(ADC)}$	ADC analog supply voltage		2.4	3.0	3.6	V
$V_{DDA(DAC)}$	DAC analog supply voltage		2.4	3.0	3.6	V
V_{DDD}	digital supply voltage		2.4	3.0	3.6	V
$I_{DDA(ADC)}$	ADC analog supply current	operating mode	–	10	–	mA
		ADC power-down	–	100	–	μA
$I_{DDA(DAC)}$	DAC analog supply current	operating mode	–	4	–	mA
		DAC power-down	–	50	–	μA
$I_{DDO(DAC)}$	DAC operational amplifier supply current	operating mode	–	2.5	–	mA
		DAC power-down	–	200	–	μA
I_{DDD}	digital supply current	operating mode	–	5	–	mA
		ADC and DAC power-down	–	300	–	μA
T_{amb}	ambient temperature		–40	–	+85	°C
Analog-to-digital converter						
$V_{i(rms)}$	input voltage (RMS value)	notes 1 and 2	–	1.0	–	V
(THD + N)/S	total harmonic distortion-plus-noise to signal ratio	at 0 dB				
		f_s = 44.1 kHz	–	–85	–80	dB
		f_s = 96 kHz	–	–80	–75	dB
		at –60 dB; A-weighted				
		f_s = 44.1 kHz	–	–36	–30	dB
		f_s = 96 kHz	–	–34	–30	dB
S/N	signal-to-noise ratio	V_i = 0 V; A-weighted				
		f_s = 44.1 kHz	90	96	–	dB
		f_s = 96 kHz	90	94	–	dB
α_{cs}	channel separation		–	100	–	dB
Digital-to-analog converter						
$V_{o(rms)}$	output voltage (RMS value)	note 3	–	900	–	mV
(THD + N)/S	total harmonic distortion plus noise-to-signal ratio	at 0 dB				
		f_s = 44.1 kHz	–	–85	–80	dB
		f_s = 96 kHz	–	–80	–71	dB
		at –60 dB; A-weighted				
		f_s = 44.1 kHz	–	–37	–30	dB
		f_s = 96 kHz	–	–35	–30	dB
α_{cs}	channel separation		–	100	–	dB
S/N	signal-to-noise ratio	code = 0; A-weighted				
		f_s = 44.1 kHz	90	100	–	dB
		f_s = 96 kHz	90	98	–	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Power performance						
P_{ADDA}	power consumption in record and playback mode		–	64	–	mW
P_{DA}	power consumption in playback only mode		–	36	–	mW
P_{AD}	power consumption in record only mode		–	46	–	mW
P_{PD}	power consumption in power-down mode		–	2.0	–	mW

Notes

1. The input voltage can be up to 2 V (RMS) when the current through the ADC input pin is limited to approximately 1 mA by using a series resistor.
2. The input voltage to the ADC scales proportionally with the power supply voltage.
3. The output voltage of the DAC scales proportionally with the power supply voltage.

BLOCK DIAGRAM

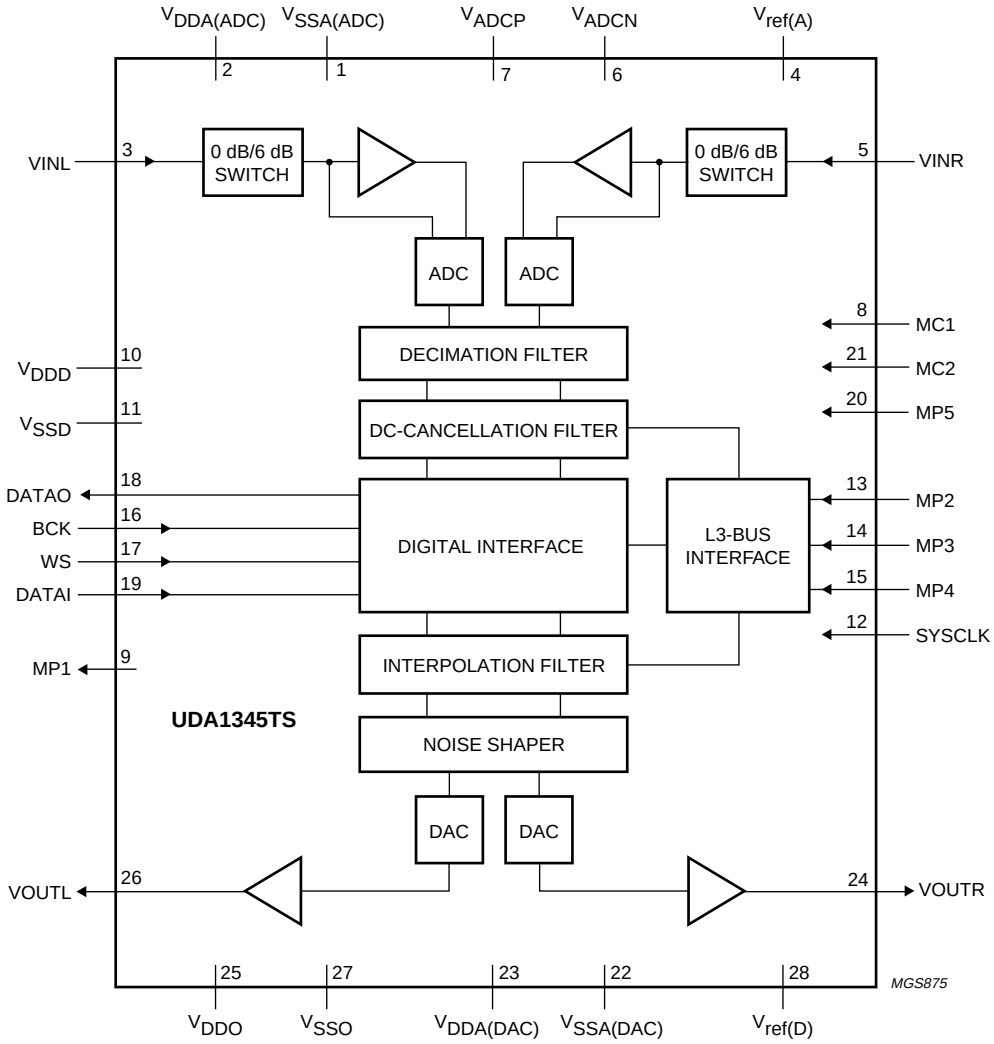


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	TYPE	DESCRIPTION
$V_{SSA(ADC)}$	1	analog ground pad	ADC analog ground
$V_{DDA(ADC)}$	2	analog supply pad	ADC analog supply voltage
VINL	3	analog input pad	ADC input left
$V_{ref(A)}$	4	analog pad	ADC reference voltage
VINR	5	analog input pad	ADC input right
V_{ADCN}	6	analog pad	ADC negative reference voltage
V_{ADCP}	7	analog pad	ADC positive reference voltage
MC1	8	5 V tolerant digital input pad with internal pull-down pad	mode control 1 (pull-down)
MP1	9	5 V tolerant slew rate controlled digital output pad	multi purpose pin 1
V_{DDD}	10	digital supply pad	digital supply voltage
V_{SSD}	11	digital ground pad	digital ground
SYSCLK	12	5 V tolerant digital Schmitt triggered input pad	system clock 256, 384 or 512f_s
MP2	13	3-level input pad	multi purpose pin 2
MP3	14	5 V tolerant digital Schmitt triggered input pad	multi purpose pin 3
MP4	15	3-level input pad	multi purpose pin 4
BCK	16	5 V tolerant digital Schmitt triggered input pad	bit clock input
WS	17	5 V tolerant digital Schmitt triggered input pad	word select input
DATAO	18	5 V tolerant slew rate controlled digital output pad	data output
DATAI	19	5 V tolerant digital Schmitt triggered input pad	data input
MP5	20	5 V tolerant digital Schmitt triggered input pad	multi purpose pin 5 (pull down)
MC2	21	5 V tolerant digital input pad with internal pull-down pad	mode control 2 (pull-down)
$V_{SSA(DAC)}$	22	analog ground pad	DAC analog ground
$V_{DDA(DAC)}$	23	analog supply pad	DAC analog supply voltage
VOUTR	24	analog output pad	DAC output right
V_{DDO}	25	analog supply pad	operational amplifier supply voltage
VOUTL	26	analog output pad	DAC output left
V_{SSO}	27	analog ground pad	operational amplifier ground
$V_{ref(D)}$	28	analog pad	DAC reference voltage

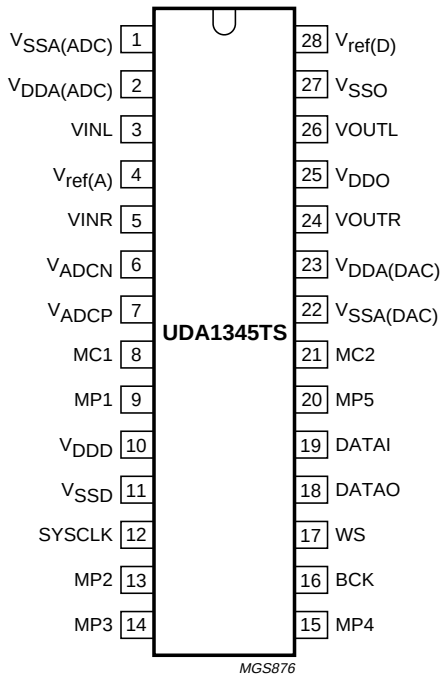


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

The UDA1345TS accommodates slave mode only, this means that in all applications the system devices must provide the system clocks (being the system clock itself and the digital audio interface signals).

The system clock must be locked in frequency to the audio digital interface input signals.

The BCK clock can be up to $128f_s$, or in other words the BCK frequency is 128 times the Word Select (WS) frequency or less: $f_{BCK} = < 128 \times f_{WS}$.

Important: the WS edge MUST fall on the negative edge of the BCK at all times for proper operation of the digital I/O data interface.

Note: the sampling frequency range is from 5 to 100 kHz, however for the $512f_s$ clock mode the sampling range is from 5 to 55 kHz.

Analog-to-Digital Converter (ADC)

The stereo ADC of the UDA1345TS consists of two 5th-order Sigma-Delta modulators. They have a modified Ritchie-coder architecture in a differential switched capacitor implementation. The oversampling ratio is 64.

Analog front-end

The analog front-end is equipped with a selectable 0 dB or 6 dB gain block (the pin to select this mode is given in Section “L3 microcontroller mode”). This block can be used in applications in which both 1 V (RMS) and 2 V (RMS) input signals can be input to the UDA1345TS.

In applications in which a 2 V (RMS) input signal is used, a 12 kΩ resistor must be used in series with the input of the ADC. This forms a voltage divider together with the internal ADC resistor and ensures that only 1 V (RMS) maximum is input to the IC. Using this application for a 2 V (RMS) input signal, the switch must be set to 0 dB. When a 1 V (RMS) input signal is input to the ADC in the same application, the gain switch must be set to 6 dB.

An overview of the maximum input voltages allowed against the presence of an external resistor and the setting of the gain switch is given in Table 1; the power supply voltage is assumed to be 3 V.

Table 1 Application modes using input gain stage

RESISTOR (12 kΩ)	INPUT GAIN SWITCH	MAXIMUM INPUT VOLTAGE
Present	0 dB	2 V (RMS)
Present	6 dB	1 V (RMS)
Absent	0 dB	1 V (RMS)
Absent	6 dB	0.5 V (RMS)

Decimation filter (ADC)

The decimation from $64f_s$ to $1f_s$ is performed in two stages.

The first stage realizes a 4th-order $\frac{\sin x}{x}$ characteristic.

This filter decreases the sample rate by 8. The second stage consists of 2 half-band filters and a recursive filter, each decimating by a factor of 2.

Table 2 Digital decimation filter characteristics

ITEM	CONDITIONS	VALUE (dB)
Pass-band ripple	$0 - 0.45f_s$	±0.05
Stop band	$>0.55f_s$	–60
Dynamic range	$0 - 0.45f_s$	114
Overall gain when a 0 dB signal is input to ADC to digital output	DC	–1.16

Note: it should be noted that the digital output level is inversely proportional to the ADC analog power supply. This means that with a constant analog input level and increasing power supply the digital output level will decrease proportionally.

Interpolation filter (DAC)

The digital filter interpolates from 1 to $128f_s$ by means of a cascade of a recursive filter and an FIR filter.

Table 3 Digital interpolation filter characteristics

ITEM	CONDITIONS	VALUE (dB)
Passband ripple	$0 - 0.45f_s$	±0.03
Stopband	$>0.55f_s$	–65
Dynamic range	$0 - 0.45f_s$	116.5
Gain	DC	–3.5

Double speed

SInce the device supports a sampling range of 8 to 100 kHz, the device can support double speed (e.g. for 44.1 kHz and 48 kHz sampling frequency) by just doubling the system speed. In double speed all features are available.

Noise shaper (DAC)

The 3rd-order noise shaper operates at $128f_s$. It shifts in-band quantization noise to frequencies well above the audio band. This noise shaping technique enables high signal-to-noise ratios to be achieved. The noise shaper output is converted into an analog signal using a filter stream digital-to-analog converter.

The Filter Stream DAC (FSDAC)

The FSDAC is a semi-digital reconstruction filter that converts the 1-bit data stream of the noise shaper to an analog output voltage. The filter coefficients are implemented as current sources and are summed at virtual ground of the output operational amplifier. In this way very high signal-to-noise performance and low clock jitter sensitivity is achieved. A post filter is not needed due to the inherent filter function of the DAC. On-board amplifiers convert the FSDAC output current to an output voltage signal capable of driving a line output.

The output voltage of the FSDAC is scaled proportionally with the power supply voltage.

Power control

In the event that the DAC is powered-up or powered-down, a cosine roll-off mute will be performed (when powering down) or a cosine roll-up de-mute (when powering up) will be performed. This is in order to prevent clicks when powering up or down. This power-on/off mute takes $32 \times 4 = 128$ samples.

L3MODE or static pin control

The UDA1345TS can be used under L3 microcontroller interface mode or under static pin control. The mode can be set via the Mode Control (MC) pins MC1 (pin 8) and MC2 (pin 21). The function of these pins is given in Table 4.

Table 4 Mode Control pins MC1 and MC2

MODE	MC2	MC1
L3MODE	LOW	LOW
Test modes	LOW	HIGH
	HIGH	LOW
Static pin mode	HIGH	HIGH

Important: in L3MODE the UDA1345TS is completely pin and function compatible with the UDA1340M and the UDA1344TS.

Note: the UDA1345TS does NOT support bass-boost and treble.

L3 microcontroller mode

The UDA1345TS is set to the L3 microcontroller mode by setting both MC1 (pin 8) and MC2 (pin 21) LOW.

The definition of the control registers is given in Section “L3 interface”.

PINNING DEFINITION

The pinning definition under L3 microcontroller interface is given in Table 5.

Table 5 Pinning definition under L3 control

SYMBOL	PIN	DESCRIPTION
MP1	9	OVERFL output
MP2	13	L3MODE input
MP3	14	L3CLOCK input
MP4	15	L3DATA input
MP5	20	ADC 1 or 2 V (RMS) input control

SYSTEM CLOCK

Under L3 control the options are 256, 384 and 512f_s.

MULTIPLE FORMAT INPUT/OUTPUT INTERFACE

The UDA1345TS supports the following data input/output formats under L3 control:

- I^2S-bus with data word length of up to 24 bits
- MSB-justified serial format with data word length of up to 20 bits
- LSB-justified serial format with data word lengths of 16, 18 or 20 bits
- Three combined data formats with MSB data output and LSB 16, 18 and 20 bits data input.

The formats are illustrated in Fig.3. Left and right data channel words are time multiplexed.

ADC INPUT VOLTAGE CONTROL

The UDA1345TS supports a 2 V (RMS) input using a series resistor of 12 kΩ as described in Section “Analog front-end”. In L3 microcontroller mode, the gain can be selected via pin MP5.

When MP5 is set LOW, 0 dB gain is selected. When MP5 is set HIGH, 6 dB gain is selected.

OVERLOAD DETECTION (ADC)

In practice the output is used to indicate whenever the output data, in either the left or right channel, is greater than −1 dB (the actual figure is −1.16 dB) of the maximum possible digital swing. When this condition is detected the OVERFL output is forced HIGH for at least 512f_s cycles (11.6 ms at f_s = 44.1 kHz). This time-out is reset for each infringement.

DC CANCELLATION FILTER (ADC)

An optional IIR high-pass filter is provided to remove unwanted DC components. The operation is selected by the microcontroller via the L3-bus. The filter characteristics are given in Table 6.

Table 6 DC cancellation filter characteristics

ITEM	CONDITIONS	VALUE (dB)
Pass-band ripple		none
Pass-band gain		0
Droop	at 0.00045f_s	0.031
Attenuation at DC	at 0.00000036f_s	>40
Dynamic range	0 – 0.45f_s	>110

Static pin mode

The UDA1345TS is set to static pin control mode by setting both MC1 (pin 8) and MC2 (pin 21) HIGH.

PINNING DEFINITION

The pinning definition under static pin control is given in Table 7.

Table 7 Pinning definition for static pin control

SYMBOL	PIN	DESCRIPTION
MP1	9	data input/output setting
MP2	13	3-level pin controlling de-emphasis and mute
MP3	14	256f_s or 384f_s system clock
MP4	15	3-level pin to control ADC power mode and 1 V (RMS) or 2 V (RMS) input
MP5	20	data input/output setting

SYSTEM CLOCK

Under static pin control the options are $256f_s$ and $384f_s$. With pin MP3 (pin 14) the mode can be set as is given in Table 8.

Table 8 System clock settings under static pin mode

MODE	MP3
$256f_s$ system clock	LOW
$384f_s$ system clock	HIGH

MUTE AND DE-EMPHASIS

Under static pin control via MP2 de-emphasis and mute can be selected for the playback path. The definition of the MP2 pin is given in Table 9.

Table 9 Settings for pin MP2

MODE	MP2
No de-emphasis and mute	LOW
De-emphasis 44.1 kHz	$0.5V_{DDD}$
Muted	HIGH

MULTIPLE FORMAT INPUT/OUTPUT INTERFACE

The data input/output formats supported under static pin control are as follows:

- I^2S-bus with data word length of up to 24 bits
- MSB-justified serial format with data word length of up to 24 bits
- Two combined data formats with MSB data output and LSB 16 and 20 bits data input.

The data formats can be selected using pins MP1 (pin 9) and MP5 (pin 20) as given in Table 10.

Table 10 Data format settings under static pin control

INPUT FORMAT	MP1	MP5
MSB mode	LOW	LOW
I^2S-bus	LOW	HIGH
MSB output LSB 20 input	HIGH	LOW
MSB output LSB 16 input	HIGH	HIGH

The formats are illustrated in Fig.3. Left and right data channel words are time multiplexed.

ADC INPUT VOLTAGE CONTROL

The UDA1345TS supports a 2 V (RMS) input using a series resistor as described in Section “Analog front-end”.

In static pin mode the 3-level pin MP4 (pin 15) is used to select 0 or 6 dB gain mode. When MP4 is set LOW the ADC is powered-down. When MP4 is set to half the power supply voltage, then 6 dB gain is selected, and when MP4 is set HIGH then 0 dB gain is selected.

Table 11 MP4 mode settings (static mode)

MODE	MP4
ADC power-down mode	LOW
6 dB gain mode	MID
0 dB gain mode	HIGH

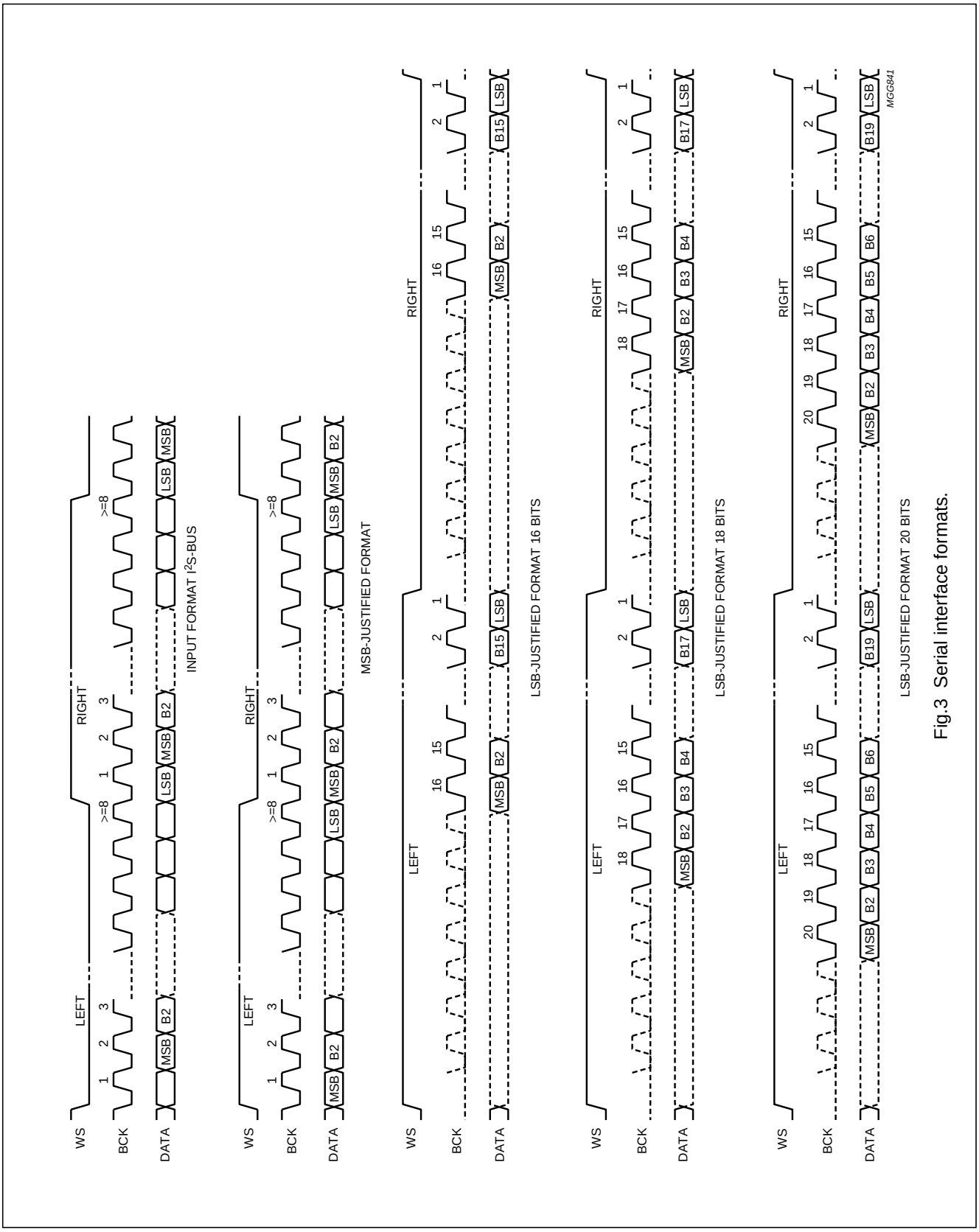


Fig.3 Serial interface formats.

L3 interface

The UDA1345TS has a microcontroller input mode. In the microcontroller mode, all of the digital sound processing features and the system controlling features can be controlled by the microcontroller. The controllable features are:

- System clock frequency
- Data input format
- Power control
- DC filtering
- De-emphasis
- Volume
- Mute.

The exchange of data and control information between the microcontroller and the UDA1345TS is accomplished through a serial hardware interface comprising the following pins:

- L3DATA: microcontroller interface data line
- L3MODE: microcontroller interface mode line
- L3CLOCK: microcontroller interface clock line.

Information transfer via the microcontroller bus is LSB first, and is organized in accordance with the so called 'L3' format, in which two different modes of operation can be distinguished; address mode and data transfer mode (see Figs 4 and 5).

The address mode is required to select a device communicating via the L3-bus and to define the destination register set for the data transfer mode. Data transfer for the UDA1345TS can only be in one direction: for the UDA1345TS, data can only be written to the device.

Important: since the UDA1345TS does not have a Power-up reset circuit, after power up the L3 interface registers MUST be initialized.

ADDRESS MODE

The address mode is used to select a device for subsequent data transfer and to define the destination register set (DATA or STATUS). The address mode is characterized by L3MODE being LOW and a burst of 8 pulses on L3CLOCK, accompanied by 8 data bits. The fundamental timing is shown in Fig.4. Data bits 0 and 1 indicate the type of subsequent data transfer as given in Table 12.

Table 12 Selection of data transfer

BIT 1	BIT 0	TRANSFER
0	0	DATA (volume, de-emphasis, mute, and power control)
0	1	not used
1	0	STATUS (system clock frequency, data input format and DC filter)
1	1	not used

Data bits 7 to 2 represent a 6-bit device address, with bit 7 being the MSB and bit 2 the LSB. The address of the UDA1345TS is 000101 (bit 7 to bit 2). In the event that the UDA1345TS receives a different address, it will deselect its microcontroller interface logic.

DATA TRANSFER MODE

The selection preformed in the address mode remains active during subsequent data transfers, until the UDA1345TS receives a new address command. The fundamental timing of data transfers is essentially the same as in the address mode, shown in Fig.4. The maximum input clock and data rate is $128f_s$. All transfers are byte wise, i.e. they are based on groups of 8 bits. Data will be stored in the UDA1345TS after the eighth bit of a byte has been received. A multibyte transfer is illustrated in Fig.6.

Programming the sound processing and other features

The feature values are stored in independent registers. The first selection of the registers is achieved by the choice of data type that is transferred, being DATA or STATUS. This is performed in the address mode, bit 1 and bit 0 (see Table 12). The second selection is performed by the 2 MSBs of the data byte (bit 7 and bit 6). The other bits in the data byte (bit 5 to bit 0) are the values that are placed in the selected registers.

When the data transfer of type DATA is selected, the features Volume, De-emphasis, Mute and Power control can be controlled. When the data transfer of type STATUS is selected, the features system clock frequency, data input format and DC filter can be controlled.

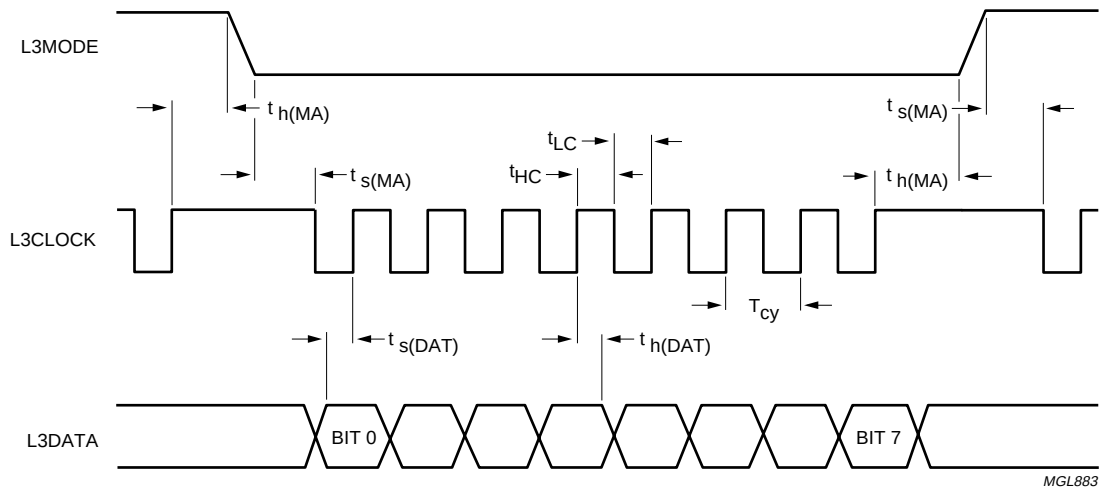


Fig.4 Timing address mode.

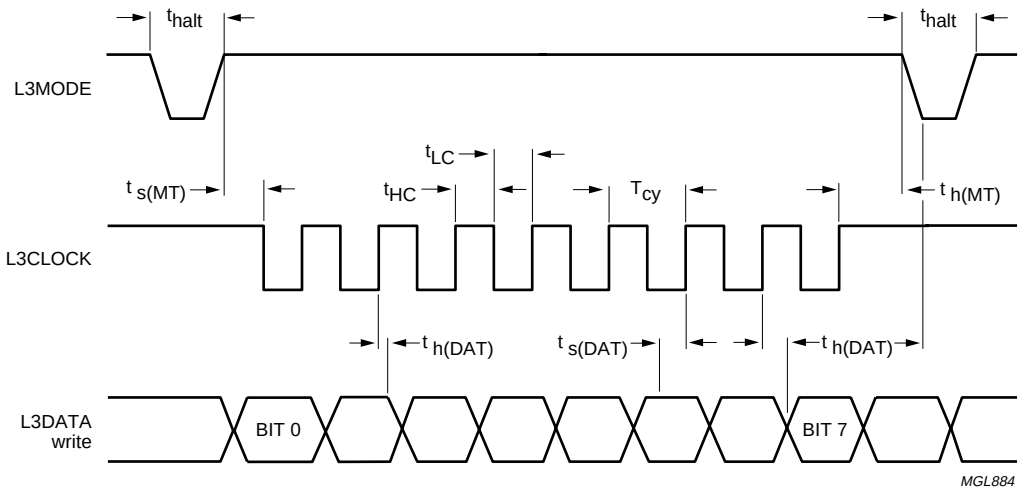


Fig.5 Timing for data transfer mode.

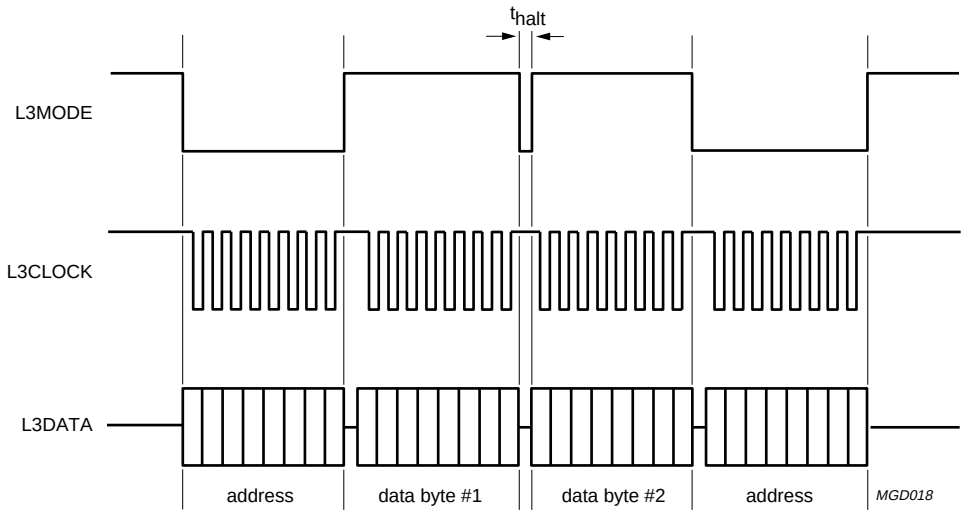


Fig.6 Multibyte transfer.

Table 13 Data transfer of type status

LAST IN TIME					FIRST IN TIME			REGISTER SELECTED
BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	
0	0	SC1	SC0	IF2	IF1	IF0	DC	System Clock frequency (5 : 4); data Input Format (3 : 1); DC-filter

Table 14 Data transfer of type data

LAST IN TIME					FIRST IN TIME			REGISTER SELECTED
BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	
0	0	VC5	VC4	VC3	VC2	VC1	VC0	Volume Control (5 : 0)
0	1	0	0	0	0	0	0	not used
1	0	0	DE1	DE0	MT	0	0	De-Emphasis (4 : 3); MuTe
1	1	0	0	0	0	PC1	PC0	Power Control (1 : 0)

System clock frequency

A 2-bit value (SC1 and SC0) to select the used external clock frequency (see Table 15).

Table 15 System clock frequency settings

SC1	SC0	FUNCTION
0	0	$512f_s$
0	1	$384f_s$
1	0	$256f_s$
1	1	not used

Data input format

A 3-bit value (IF2 to IF0) to select the used data format (see Table 16).

Table 16 Data input format settings

IF2	IF1	IF0	FUNCTION
0	0	0	I^2S-bus
0	0	1	LSB-justified; 16 bits
0	1	0	LSB-justified; 18 bits
0	1	1	LSB-justified; 20 bits
1	0	0	MSB-justified
1	0	1	MSB-justified output/ LSB-justified 16 bits input
1	1	0	MSB-justified output/ LSB-justified 18 bits input
1	1	1	MSB-justified output/ LSB-justified 20 bits input

DC filter

A 1-bit value to enable the digital DC filter (see Table 17).

Table 17 DC filtering

DC	FUNCTION
0	no DC filtering
1	DC filtering

Volume control

A 6-bit value to program the left and right channel volume attenuation (VC5 to VC0). The range is 0 dB to –∞ dB in steps of 1 dB (see Table 18).

Table 18 Volume settings

VC5	VC4	VC3	VC2	VC1	VC0	VOLUME (dB)
0	0	0	0	0	0	0
0	0	0	0	0	1	0
0	0	0	0	1	0	–1
0	0	0	0	1	1	–2
:	:	:	:	:	:	:
1	1	0	0	1	1	–50
1	1	0	1	0	0	–52
1	1	0	0	0	1	–54
1	1	0	0	1	0	–57
1	1	0	1	1	1	–60
1	1	1	0	0	0	–66
1	1	1	0	0	1	–∞
:	:	:	:	:	:	:
1	1	1	1	1	1	–∞

De-emphasis

A 2-bit value to enable the digital de-emphasis filter.

Table 19 De-emphasis settings

DE1	DE0	FUNCTION
0	0	no de-emphasis
0	1	de-emphasis; 32 kHz
1	0	de-emphasis; 44.1 kHz
1	1	de-emphasis; 48 kHz

Mute

A 1-bit value to enable the digital DAC mute (playback).

Table 20 DAC mute

MT	FUNCTION
0	no muting
1	muting

Power control

A 2-bit value to disable the ADC and/or DAC to reduce power consumption.

Table 21 Power control settings

PC1	PC0	FUNCTION	
		ADC	DAC
0	0	off	off
0	1	off	on
1	0	on	off
1	1	on	on

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134). All voltages referenced to ground; $V_{DDD} = V_{DDA} = V_{DDO} = 3$ V; $T_{amb} = 25$ °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DDD}	digital supply voltage	note 1	–	5.0	V
$T_{xtal(max)}$	maximum crystal temperature		–	150	°C
T_{stg}	storage temperature		–65	+125	°C
T_{amb}	ambient temperature		–40	+85	°C
V_{es}	electrostatic handling	according to JEDEC II specification			
$I_{lu(prot)}$	latch-up protection current	$T_{amb} = 125$ °C; $V_{DD} = 3.6$ V	–	200	mA
$I_{sc(DAC)}$	short-circuit current of DAC	$T_{amb} = 0$ °C; $V_{DD} = 3$ V; note 2			
		output short-circuited to $V_{SSA(DAC)}$	–	450	mA
		output short-circuited to $V_{DDA(DAC)}$	–	325	mA

Notes

1. All V_{DD} and V_{SS} connections must be made to the same power supply.
2. DAC operation after short-circuiting cannot be warranted.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	90	K/W

DC CHARACTERISTICS

$V_{DDD} = V_{DDA} = V_{DDO} = 3.0$ V; $f_s = 44.1$ kHz; $T_{amb} = 25$ °C; $R_L = 5$ kΩ; note 1; all voltages referenced to ground (pins 1, 11, 22 and 27); unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies						
$V_{DDA(ADC)}$	ADC analog supply voltage		2.4	3.0	3.6	V
$V_{DDA(DAC)}$	DAC analog supply voltage		2.4	3.0	3.6	V
V_{DDD}	digital supply voltage		2.4	3.0	3.6	V
$I_{DDA(ADC)}$	ADC analog supply current	operating mode	–	10	–	mA
		ADC power-down	–	100	–	μA
$I_{DDA(DAC)}$	DAC analog supply current	operating mode	–	4	–	mA
		DAC power-down	–	50	–	μA
$I_{DDO(DAC)}$	DAC operational amplifier supply current	operating mode	–	2.5	–	mA
		DAC power-down	–	200	–	μA
I_{DDD}	digital supply current	operating mode	–	5.0	–	mA
		ADC and DAC power-down	–	300	–	μA
Digital input pins (5V tolerant TTL compatible)						
V_{IH}	HIGH-level input voltage		2.0	–	5.0	V
V_{IL}	LOW-level input voltage		–0.5	–	0.8	V
$V_{IH(th)}$	HIGH-level threshold input voltage		1.3	–	1.9	V
$V_{IL(th)}$	LOW-level threshold input voltage		0.9	–	1.35	V
V_{hys}	Schmitt trigger hysteresis voltage		0.4	–	0.7	V
$\lvert I_{LI} \rvert$	input leakage current		–	–	10	μA
C_i	input capacitance		–	–	10	pF
3-level input pins (MP2; MP4)						
V_{IH}	HIGH-level input voltage		$0.9V_{DDD}$	–	$V_{DDD} + 0.5$	V
V_{IM}	MIDDLE-level input voltage		$0.4V_{DDD}$	–	$0.6V_{DDD}$	V
V_{IL}	LOW-level input voltage		–0.5	–	+0.5	V
Digital output pins						
V_{OH}	HIGH-level output voltage	$I_{OH} = -2$ mA	$0.85V_{DDD}$	–	–	V
V_{OL}	LOW-level output voltage	$I_{OL} = 2$ mA	–	–	0.4	V
Analog-to-digital converter						
$V_{ref(A)}$	reference voltage	with respect to V_{SSA}	$0.45V_{DDA}$	$0.5V_{DDA}$	$0.55V_{DDA}$	V
$R_{o(ref)}$	$V_{ref(A)}$ reference output resistance		–	24	–	kΩ
R_i	input resistance	$f_i = 1$ kHz	–	12	–	kΩ
C_i	input capacitance		–	20	–	pF

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Digital-to-analog converter						
$V_{ref(D)}$	reference voltage	with respect to V_{SSA}	$0.45V_{DDA}$	$0.5V_{DDA}$	$0.55V_{DDA}$	V
$R_{o(ref)}$	$V_{ref(D)}$ reference output resistance		–	12.5	–	kΩ
R_o	DAC output resistance		–	0.13	3.0	Ω
$I_{o(max)}$	maximum output current	(THD + N)/S < 0.1%; R_L = 800 Ω	–	tbf	–	mA
R_L	load resistance		3	–	–	kΩ
C_L	load capacitance	note 2	–	–	200	pF

Notes

1. All power supply pins (V_{DD} and V_{SS}) must be connected to the same external power supply unit.
2. When higher capacitive loads must be driven then a 100 Ω resistor must be connected in series with the DAC output in order to prevent oscillations in the output operational amplifier.

AC CHARACTERISTICS (ANALOG)

$V_{DDD} = V_{DDA} = V_{DDO} = 3.0$ V; $f_i = 1$ kHz; $f_s = 44.1$ kHz; $T_{amb} = 25$ °C; $R_L = 5$ kΩ; all voltages referenced to ground (pins 1, 11, 22 and 27); unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Analog-to-digital converter						
$V_{i(rms)}$	input voltage (RMS value)	notes 1 and 2	–	1.0	–	V
ΔV_i	unbalance between channels		–	0.1	–	dB
(THD + N)/S	total harmonic distortion plus noise-to-signal ratio	at 0 dB				
		$f_s = 44.1$ kHz	–	–85	–80	dB
		$f_s = 96$ kHz	–	–80	–75	dB
		at –60 dB; A-weighted				
		$f_s = 44.1$ kHz	–	–36	–30	dB
		$f_s = 96$ kHz	–	–34	–30	dB
S/N	signal-to-noise ratio	$V_i = 0$ V; A-weighted				
		$f_s = 44.1$ kHz	90	96	–	dB
		$f_s = 96$ kHz	90	94	–	dB
α_{cs}	channel separation		–	100	–	dB
PSRR	power supply rejection ratio	$f_{ripple} = 1$ kHz; $V_{ripple(p-p)} = 1\%$	–	30	–	dB
Digital-to-analog converter						
$V_{o(rms)}$	output voltage (RMS value)	note 3	–	900	–	mV
ΔV_o	unbalance between channels		–	0.1	–	dB
(THD + N)/S	total harmonic distortion plus noise-to-signal ratio	at 0 dB				
		$f_s = 44.1$ kHz	–	–85	–80	dB
		$f_s = 96$ kHz	–	–80	–71	dB
		at –60 dB; A-weighted				
		$f_s = 44.1$ kHz	–	–37	–30	dB
		$f_s = 96$ kHz	–	–35	–30	dB
S/N	signal-to-noise ratio	code = 0; A-weighted				
		$f_s = 44.1$ kHz	90	100	–	dB
		$f_s = 96$ kHz	90	98	–	dB
α_{cs}	channel separation		–	100	–	dB
PSRR	power supply rejection ratio	$f_{ripple} = 1$ kHz; $V_{ripple(p-p)} = 1\%$	–	60	–	dB

Notes

1. The input voltage can be up to 2 V (RMS) when the current through the ADC input pin is limited to approximately 1 mA by using a series resistor.
2. The input voltage to the ADC scales proportionally with the power supply voltage.
3. The output voltage of the DAC scales proportionally with the power supply voltage.

AC CHARACTERISTICS (DIGITAL)

V_{DDD} = V_{DDA} = V_{DDO} = 2.7 to 3.6 V; T_{amb} = −20 to +85 °C; R_L = 5 kΩ; all voltages referenced to ground (pins 1, 11, 22 and 27); unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
System clock timing; see Fig.7						
T_{sys}	system clock cycle	$f_{sys} = 256f_s$; note 1	39	88	781	ns
		$f_{sys} = 384f_s$; note 1	26	59	520	ns
		$f_{sys} = 512f_s$; note 2	36	44	390	ns
t_{CWL}	f_{sys} LOW-level pulse width	f_{sys} < 19.2 MHz	$0.30T_{sys}$	–	$0.70T_{sys}$	ns
		$f_{sys} \geq$ 19.2 MHz	$0.40T_{sys}$	–	$0.60T_{sys}$	ns
t_{CWH}	f_{sys} HIGH-level pulse width	f_{sys} < 19.2 MHz	$0.30T_{sys}$	–	$0.70T_{sys}$	ns
		$f_{sys} \geq$ 19.2 MHz	$0.40T_{sys}$	–	$0.60T_{sys}$	ns
t_r	rise time		–	–	20	ns
t_f	fall time		–	–	20	ns
Serial input/output data timing; see Fig.8						
t_{BCK}	bit clock period		$1/128f_s$	–	–	ns
t_{BCKH}	bit clock HIGH time		34	–	–	ns
t_{BCKL}	bit clock LOW time		34	–	–	ns
t_r	rise time		–	–	20	ns
t_f	fall time		–	–	20	ns
$t_{s(DATAI)}$	data input set-up time		20	–	–	ns
$t_{h(DATAI)}$	data input hold time		0	–	–	ns
$t_{d(DATAO-BCK)}$	data output delay time (from BCK falling edge)		–	–	80	ns
$t_{d(DATAO-WS)}$	data output delay time (from WS edge)	MSB-justified format	–	–	80	ns
$t_{h(DATAO)}$	data output hold time		0	–	–	ns
$t_{s(WS)}$	word select set-up time		20	–	–	ns
$t_{h(WS)}$	word select hold time		10	–	–	ns
Address and data transfer mode timing; see Figs 4 and 5						
T_{cy}	L3CLOCK cycle time		500	–	–	ns
t_{HC}	L3CLOCK HIGH period		250	–	–	ns
t_{LC}	L3CLOCK LOW period		250	–	–	ns
$t_{s(MA)}$	L3MODE set-up time	address mode	190	–	–	ns
$t_{h(MA)}$	L3MODE hold time	address mode	190	–	–	ns
$t_{s(MT)}$	L3MODE set-up time	data transfer mode	190	–	–	ns
$t_{h(MT)}$	L3MODE hold time	data transfer mode	190	–	–	ns

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$t_{s(DAT)}$	L3DATA set-up time	data transfer mode and address mode	190	–	–	ns
$t_{h(DAT)}$	L3DATA hold time	data transfer mode and address mode	30	–	–	ns
t_{halt}	L3MODE halt time		190	–	–	ns

Notes

1. Sampling range from 5 to 100 kHz is supported, with f_s = 44.1 kHz typical.
2. Sampling range from 5 to 55 kHz is supported, with f_s = 44.1 kHz typical.

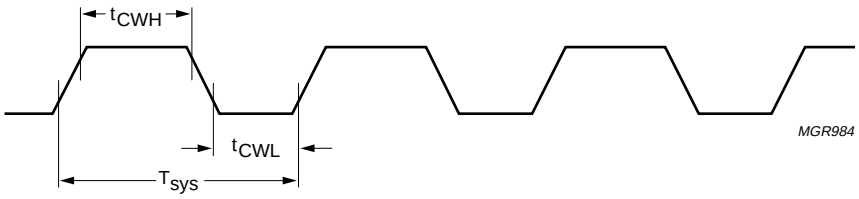


Fig.7 System clock timing.

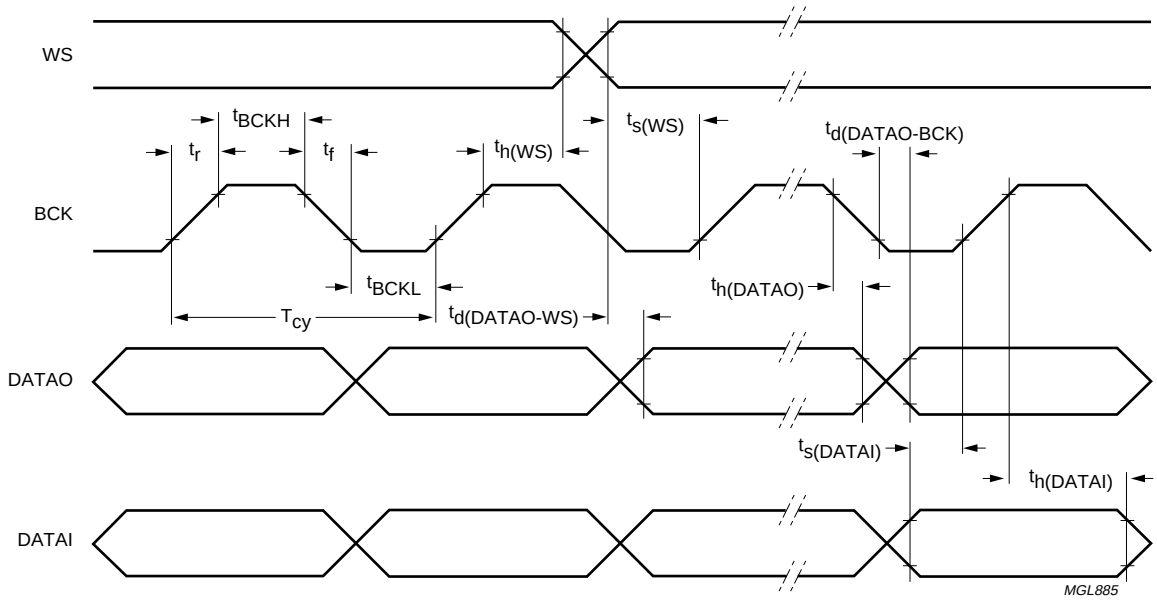


Fig.8 Serial interface timing.

APPLICATION INFORMATION

The application information as given in Fig.9, is an optimum application environment. Simplification is possible at the cost of some performance degradation. The following notes apply:

- The capacitors at the output of the DAC can be reduced. It should be noted that the cut-off frequency of the DC filter also changes.
- The capacitors at the input of the ADC can also be reduced. It should be noted that the cut-off frequency of the capacitor with the 12 kΩ input resistance of the ADC will also change.

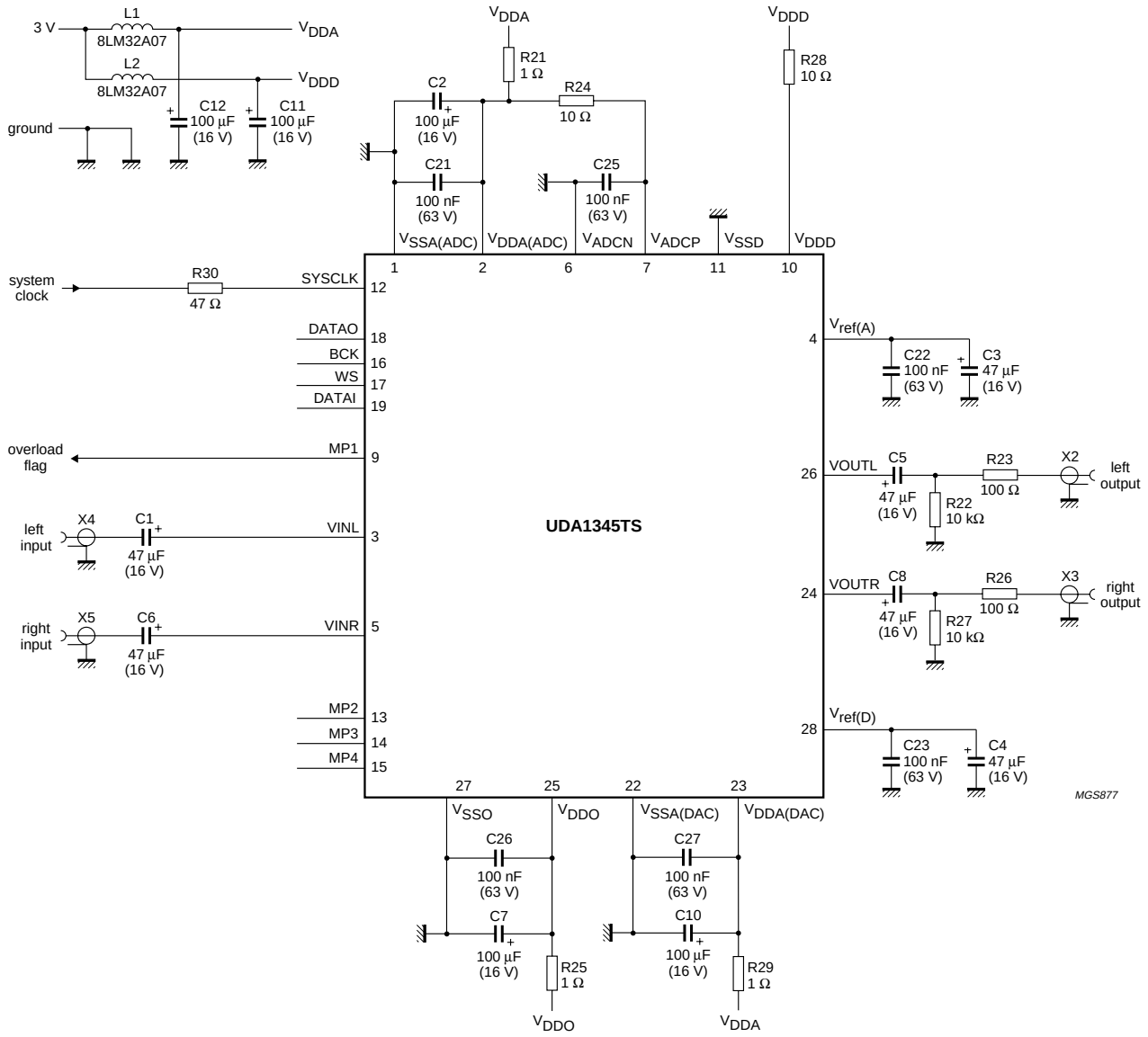
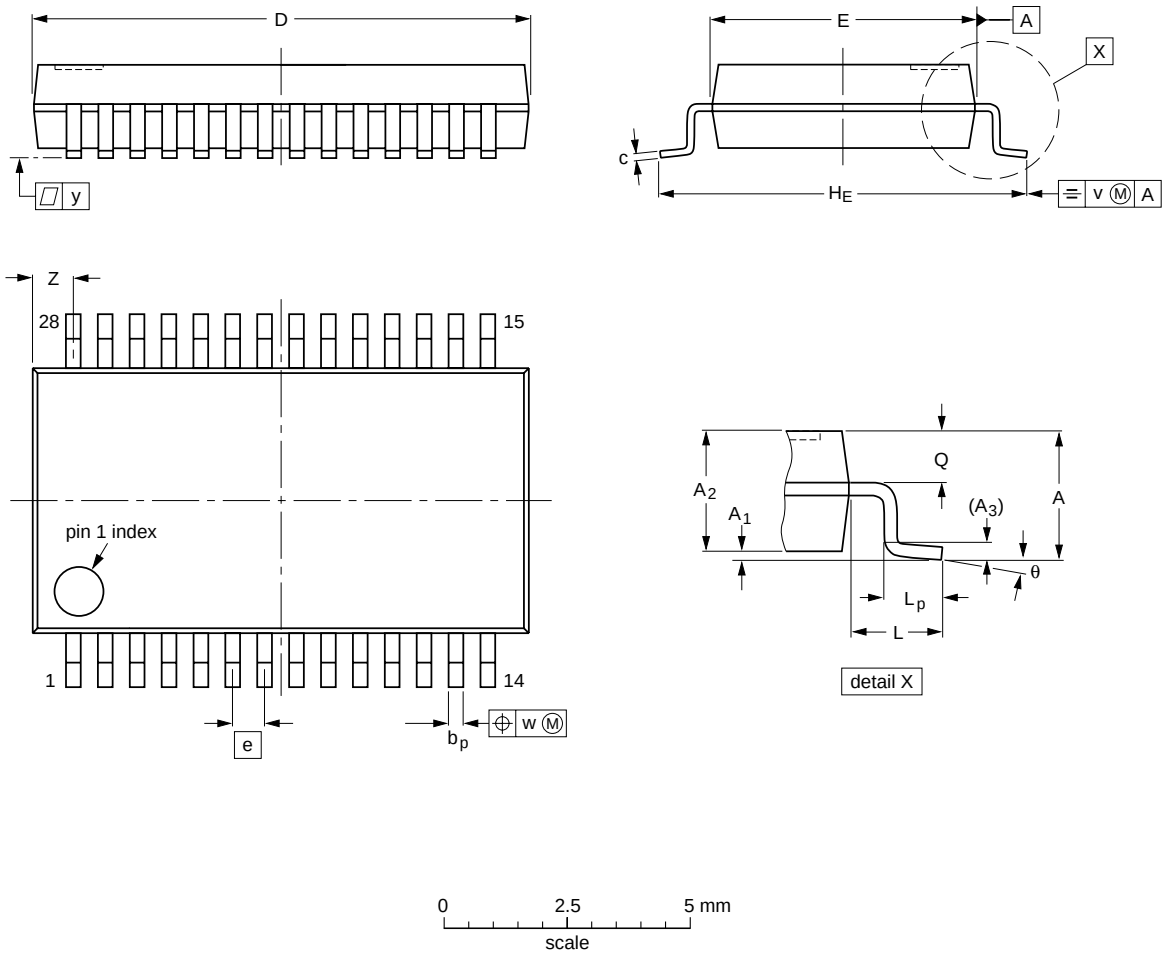


Fig.9 Application diagram.

PACKAGE OUTLINE

SSOP28: plastic shrink small outline package; 28 leads; body width 5.3 mm **SOT341-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2.0	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	10.4 10.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	1.1 0.7	8^o 0^o

Note

1. Plastic or metal protrusions of 0.20 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT341-1		MO-150				~~95-02-04~~ 99-12-27

SOLDERING

Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering is not always suitable for surface mount ICs, or for printed-circuit boards with high population densities. In these situations reflow soldering is often used.

Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, infrared/convection heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 250 °C. The top-surface temperature of the packages should preferable be kept below 230 °C.

Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
  - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

  The footprint must incorporate solder thieves at the downstream end.
- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time is 4 seconds at 250 °C.
A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

Suitability of surface mount IC packages for wave and reflow soldering methods

PACKAGE	SOLDERING METHOD	
	WAVE	REFLOW(1)
BGA, LFBGA, SQFP, TFBGA	not suitable	suitable
HBCC, HLQFP, HSQFP, HSOP, HTQFP, HTSSOP, SMS	not suitable(2)	suitable
PLCC(3), SO, SOJ	suitable	suitable
LQFP, QFP, TQFP	not recommended(3)(4)	suitable
SSOP, TSSOP, VSO	not recommended(5)	suitable

Notes

1. All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *"Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods"*.
2. These packages are not suitable for wave soldering as a solder joint between the printed-circuit board and heatsink (at bottom version) can not be achieved, and as solder may stick to the heatsink (on top version).
3. If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.
4. Wave soldering is only suitable for LQFP, TQFP and QFP packages with a pitch (e) equal to or larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.
5. Wave soldering is only suitable for SSOP and TSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

DATA SHEET STATUS

DATA SHEET STATUS	PRODUCT STATUS	DEFINITIONS [1]
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
Preliminary specification	Qualification	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
Product specification	Production	This data sheet contains final specifications. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.

Note

1. Please consult the most recently issued data sheet before initiating or completing a design.

DEFINITIONS

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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NOTES

Philips Semiconductors – a worldwide company

Argentina: see South America

Australia: 3 Figtree Drive, HOMEBUSH, NSW 2140,
Tel. +61 2 9704 8141, Fax. +61 2 9704 8139

Austria: Computerstr. 6, A-1101 WIEN, P.O. Box 213,
Tel. +43 1 60 101 1248, Fax. +43 1 60 101 1210

Belarus: Hotel Minsk Business Center, Bld. 3, r. 1211, Volodarski Str. 6,
220050 MINSK, Tel. +375 172 20 0733, Fax. +375 172 20 0773

Belgium: see The Netherlands

Brazil: see South America

Bulgaria: Philips Bulgaria Ltd., Energoproject, 15th floor,
51 James Bourchier Blvd., 1407 SOFIA,
Tel. +359 2 68 9211, Fax. +359 2 68 9102

Canada: PHILIPS SEMICONDUCTORS/COMPONENTS,
Tel. +1 800 234 7381, Fax. +1 800 943 0087

China/Hong Kong: 501 Hong Kong Industrial Technology Centre,
72 Tat Chee Avenue, Kowloon Tong, HONG KONG,
Tel. +852 2319 7888, Fax. +852 2319 7700

Colombia: see South America

Czech Republic: see Austria

Denmark: Sydhavnsgade 23, 1780 COPENHAGEN V,
Tel. +45 33 29 3333, Fax. +45 33 29 3905

Finland: Sinikalliontie 3, FIN-02630 ESPOO,
Tel. +358 9 615 800, Fax. +358 9 6158 0920

France: 51 Rue Carnot, BP317, 92156 SURESNES Cedex,
Tel. +33 1 4099 6161, Fax. +33 1 4099 6427

Germany: Hammerbrookstraße 69, D-20097 HAMBURG,
Tel. +49 40 2353 60, Fax. +49 40 2353 6300

Hungary: see Austria

India: Philips INDIA Ltd, Band Box Building, 2nd floor,
254-D, Dr. Annie Besant Road, Worli, MUMBAI 400 025,
Tel. +91 22 493 8541, Fax. +91 22 493 0966

Indonesia: PT Philips Development Corporation, Semiconductors Division,
Gedung Philips, Jl. Buncit Raya Kav.99-100, JAKARTA 12510,
Tel. +62 21 794 0040 ext. 2501, Fax. +62 21 794 0080

Ireland: Newstead, Clonskeagh, DUBLIN 14,
Tel. +353 1 7640 000, Fax. +353 1 7640 200

Israel: RAPAC Electronics, 7 Kehilat Saloniki St, PO Box 18053,
TEL AVIV 61180, Tel. +972 3 645 0444, Fax. +972 3 649 1007

Italy: PHILIPS SEMICONDUCTORS, Via Casati, 23 - 20052 MONZA (MI),
Tel. +39 039 203 6838, Fax +39 039 203 6800

Japan: Philips Bldg 13-37, Kohnan 2-chome, Minato-ku,
TOKYO 108-8507, Tel. +81 3 3740 5130, Fax. +81 3 3740 5057

Korea: Philips House, 260-199 Itaewon-dong, Yongsan-ku, SEOUL,
Tel. +82 2 709 1412, Fax. +82 2 709 1415

Malaysia: No. 76 Jalan Universiti, 46200 PETALING JAYA, SELANGOR,
Tel. +60 3 750 5214, Fax. +60 3 757 4880

Mexico: 5900 Gateway East, Suite 200, EL PASO, TEXAS 79905,
Tel. +9-5 800 234 7381, Fax +9-5 800 943 0087

Middle East: see Italy

Netherlands: Postbus 90050, 5600 PB EINDHOVEN, Bldg. VB,
Tel. +31 40 27 82785, Fax. +31 40 27 88399

New Zealand: 2 Wagener Place, C.P.O. Box 1041, AUCKLAND,
Tel. +64 9 849 4160, Fax. +64 9 849 7811

Norway: Box 1, Manglerud 0612, OSLO,
Tel. +47 22 74 8000, Fax. +47 22 74 8341

Pakistan: see Singapore

Philippines: Philips Semiconductors Philippines Inc.,
106 Valero St. Salcedo Village, P.O. Box 2108 MCC, MAKATI,
Metro MANILA, Tel. +63 2 816 6380, Fax. +63 2 817 3474

Poland: Al.Jerozolimskie 195 B, 02-222 WARSAW,
Tel. +48 22 5710 000, Fax. +48 22 5710 001

Portugal: see Spain

Romania: see Italy

Russia: Philips Russia, Ul. Usatcheva 35A, 119048 MOSCOW,
Tel. +7 095 755 6918, Fax. +7 095 755 6919

Singapore: Lorong 1, Toa Payoh, SINGAPORE 319762,
Tel. +65 350 2538, Fax. +65 251 6500

Slovakia: see Austria

Slovenia: see Italy

South Africa: S.A. PHILIPS Pty Ltd., 195-215 Main Road Martindale,
2092 JOHANNESBURG, P.O. Box 58088 Newville 2114,
Tel. +27 11 471 5401, Fax. +27 11 471 5398

South America: Al. Vicente Pinzon, 173, 6th floor,
04547-130 SÃO PAULO, SP, Brazil,
Tel. +55 11 821 2333, Fax. +55 11 821 2382

Spain: Balmes 22, 08007 BARCELONA,
Tel. +34 93 301 6312, Fax. +34 93 301 4107

Sweden: Kottbygatan 7, Akalla, S-16485 STOCKHOLM,
Tel. +46 8 5985 2000, Fax. +46 8 5985 2745

Switzerland: Allmendstrasse 140, CH-8027 ZÜRICH,
Tel. +41 1 488 2741 Fax. +41 1 488 3263

Taiwan: Philips Semiconductors, 6F, No. 96, Chien Kuo N. Rd., Sec. 1,
TAIPEI, Taiwan Tel. +886 2 2134 2886, Fax. +886 2 2134 2874

Thailand: PHILIPS ELECTRONICS (THAILAND) Ltd.,
209/2 Sanpavuth-Bangna Road Prakanong, BANGKOK 10260,
Tel. +66 2 745 4090, Fax. +66 2 398 0793

Turkey: Yukari Dudullu, Org. San. Blg., 2.Cad. Nr. 28 81260 Umraniye,
ISTANBUL, Tel. +90 216 522 1500, Fax. +90 216 522 1813

Ukraine: PHILIPS UKRAINE, 4 Patrice Lumumba str., Building B, Floor 7,
252042 KIEV, Tel. +380 44 264 2776, Fax. +380 44 268 0461

United Kingdom: Philips Semiconductors Ltd., 276 Bath Road, Hayes,
MIDDLESEX UB3 5BX, Tel. +44 208 730 5000, Fax. +44 208 754 8421

United States: 811 East Arques Avenue, SUNNYVALE, CA 94088-3409,
Tel. +1 800 234 7381, Fax. +1 800 943 0087

Uruguay: see South America

Vietnam: see Singapore

Yugoslavia: PHILIPS, Trg N. Pasica 5/v, 11000 BEOGRAD,
Tel. +381 11 3341 299, Fax.+381 11 3342 553

For all other countries apply to: Philips Semiconductors,
International Marketing & Sales Communications, Building BE-p, P.O. Box 218,
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Internet: http://www.semiconductors.philips.com

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